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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,664	03/17/2004	Shawn D. Rogers	10599/130	2665

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BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610

EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,664	ROGERS ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/18/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) *8-47,49-51,55-57 and 61-71* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,48,52-54 and 58-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/21/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The preliminary amendment filed on 08/18/2006 has been entered.

Election/Restriction

2. Applicants' election without traverse of species VI (shown in figure 8 and paragraph 59) in the reply filed on 8/18/06 is acknowledged. Per Applicants' request, claims 8-42 and 45-47 are withdrawn from consideration. It is noted that the species VI invention does not include the second capacitors of claims 49, 50, and 55-57, the PCB of claims 43 and 44, or the PDN of claims 51 and 61-71. For this reason, claims 43 and 44, 49, 50, 51, 55-57, and 61-71 are also withdrawn from consideration.

Oath/Declaration

3. In a paper received 10/12/2004, Applicants petitioned for 37 CFR 1.47(a) (missing, non-signing inventor) status. Applicants' petition was granted 11/09/04. Subject to the conditions laid out in Rule 1.47(a) and the 11/09/04 petition decision, the oath/ declaration received 10/12/2004 is acceptable.

Drawings

4. The formal drawings filed on 03/17/2004 are acceptable.

Priority

5. Applicants have made no claim for priority.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 03/21/2005 has been considered.

Claim Objections

7. Claim 48 is objected to because of the following informalities:

In line 9 of claim 48, an element is introduced as "a conductive rod pair." Line 11, at least from appearances, introduces a second element to be known as "a conductive rod pair."

A claim that claims two different elements, and refers to both by the same name, is indefinite because the reader never knows which of the two elements is referred to when that name is used.

It is assumed Applicants meant to write "said rod pair" in line 11.

In line 12 of claim 48, there is no antecedent basis for "the rod pairs." There is antecedent basis for one of "the rod pairs," but there is no antecedent basis for the rest of them.

Claim 48 will be examined on the assumption that Applicants intended to it to read:

> 48. (New) An apparatus for suppressing noise in an electrical device, the apparatus comprising:
> a first conductive layer;
> a second conductive layer separated from the first conductive layer;
> a plurality of conductive rod pairs disposed in a locally periodic or nearly periodic pattern; and

a first capacitor connecting a proximate end of
a first conductive rod and
a second conductive rod;
said first conductive rod being connected to the first conductive layer and traversing the second conductive layer; said second conductive rod being connected to the second conductive layer and traversing the first conductive layer, wherein the first conductive rod and the second conductive rod are disposed adjacent to each other and form
one of said plurality of conductive rod pairs.

8. Claim 54 is objected to because there is no apparent antecedent basis for "the printed circuit board," recited in line 2 of claim 54. There is a multilayer the printed circuit board in claim 53, but claim 54 does not depend from 53.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-4, 7, 48, 52-54, and 58-60 are rejected under 35 U.S.C. 102(b) as being anticipated by HERNANDEZ (RE35,064).

With regard to claims 1-4 and 7 Hernandez discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 132; a second conductive layer 98 (the second conductive layer is visible, but not numbered, in figure 13. It is the conductive layer separated from lattice 124 by a first dielectric layer 92, also not numbered in figure 13 but numbered 12 (figure 9 shows numeral 12, but that part is referred to in figure 10 and the written description as dielectric layer 92. The written description does not refer to a part #12 in figure 9) in figure 9. Since figure 9 uses part #98 to refer to the second conductive layer, and figure 13 uses no part #, the second conductive layer will be referred to, for convenience, as part #98) separated from first conductive layer 132; first conductive rods 120 (not numbered in figure 13, the same part is numbered 120 in figure 12) comprising plated vias passing through a first dielectric layer 92 (see the discussion above concerning second conductive layer 98. The first dielectric layer is shown without reference # in figure 13, referenced as part #12 in figure 9, and discussed in the written description as part #92) disposed between the first 132 and second 98 conductive layers, connected to the second conductive layer 98, and extending to the first conductive layer 132; and chip capacitors 102 arrayed over substantially an entire area of the first conductive layer 132, connecting the first conductive rods 120 to the first conductive layer 132, and arranged in a lattice 124. Note figures 7-10 and 13 (note that figure 13 employs two lattices 124 and 126 of the sort shown in detail in figure 9 as lattice 96, said lattice 96 being identified as a lattice 44 of chip capacitors 102 in figures 6-8, the construction of said lattice 44 being

detailed in figures 6-8.The rectangular lattice of chips 102 is best seen in cutaway figure 10), column 5 lines 19-36, column 6 lines 2-24 and 65-67, and column 7 lines 1-8 of Hernandez.

With regard to claims 48, 52-54,58,59, and 60 Hernandez discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 132 of a multilayered printed circuit board; a second conductive layer 98 (the second conductive layer is visible, but not numbered, in figure 12. It is the conductive layer separated from lattice 124 by a first dielectric layer 92, also not numbered in figure 13 but numbered 12 (figure 9 shows numeral 12, but that part is referred to in figure 10 and the written description as dielectric layer 92. The written description does not refer to a part #12 in figure 9) in figure 9. Since figure 9 uses part #98 to refer to the second conductive layer, and figure 12 uses no part #, the second conductive layer will be referred to, for convenience, as part #98) of said multilayered printed circuit board separated from the first conductive layer 132; a plurality of conductive rod pairs 118-120 disposed in a rectangular periodic pattern; and a first chip capacitor 102 disposed on an outer surface of the printed circuit board and connecting a proximate end of a first conductive rod 120 and a second conductive rod 118; said first conductive rod 120 being connected to the first conductive layer 132 and traversing the second conductive layer 98; said second conductive rod 118 being connected to the second conductive layer 98 and traversing the first conductive layer 132, wherein the first conductive rod 120 and the second conductive rod 118 are disposed adjacent to each other and form one of said plurality of

conductive rod pairs 118-120. Note figures 7-10 and 12 (note that figure 12 employs lattice 96 as shown in detail in figure 9, said lattice 96 being identified as a lattice 44 of chip capacitors 102 in figures 6-8, the construction of said lattice 44 being detailed in figures 6-8.The rectangular lattice of chips 102 is best seen in cutaway figure 10), column 5 lines 19-36, column 6 lines 2-24 and 65-67, and column 7 lines 1-8 of Hernandez.

The applicant's claims 59 and 60 do not distinguish over the Hernandez reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of accommodating circuit components and accommodating signal and ground connections.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. See *In re Ludtke and Sloan*, 169 USPQ 563 at 567, and *In re Swinehart* 169 USPQ 226, both of which make it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also In re Schreiber, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997), for a discussion of the roles of examiner and applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

B. Claims 1-7, 48, 52-54, and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by MCKINZIE III (6,476,771).

With regard to claims 1-7 McKinzie III discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 903; a second conductive layer 901 separated from the first conductive layer 903; a third conductive layer 905 disposed on an opposite side of the second conductive layer 901 as the first conductive layer 903; a first dielectric layer 912 disposed between the first conductive layer 903 and the second conductive layer 901, connected to the second conductive layer 901, and extending to the first conductive layer 903; a second dielectric layer 913 disposed between the second conductive layer 901 and the third conductive layer 905 and extending to the third conductive layer 905; first conductive rods 922 or 924 comprising plated vias passing through said first dielectric layer 912 disposed between the first 903 and second 901 conductive layers and passing through said second dielectric layer 913; and chip capacitors 911 and 914 (McKinzie III refers to the chip capacitors 911 and 914 as "capacitive frequency selective surface (FSS) capacitors") arrayed over substantially an entire area of the first conductive layer 903, arranged in a lattice on the first conductive layer 903 and the third conductive layer 905, and connecting the first conductive rods 922 or 924 to the first conductive layer 903 and the third conductive layer 905. Note figures 9A-9B and column 5 lines 10-67 of McKinzie III.

With regard to claims 48, 52-54, and 58, McKinzie III discloses an apparatus for suppressing noise in an electrical device comprising a first conductive layer 903 of a

multilayered printed circuit board 900; a second conductive layer 901 of said multilayered printed circuit board 900 separated from the first conductive layer 903; a plurality of conductive rod pairs 921-922 disposed in a rectangular periodic pattern (see fig. 9B); and a first chip capacitor 911 (McKinzie III refers to the chip capacitors 911 and 914 as a "capacitive frequency selective surface (FSS) capacitor") disposed on an outer surface of the printed circuit board 900 and connecting a proximate end of a first conductive rod 922 and a second conductive rod 921; said first conductive rod 922 being connected to the first conductive layer 903 and traversing the second conductive layer 901; said second conductive rod 921 being connected to the second conductive layer 901 and traversing the first conductive layer 903, wherein the first conductive rod 922 and the second conductive rod 921 are disposed adjacent to each other and form one of said plurality of conductive rod pairs. Note figures 9A-9B and column 5 lines 10-67 of McKinzie III.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Primary Examiner
Art Unit 2826